SPECIFICATION AMENDMENTS

Replace the paragraph beginning at page 1, line 12 with:

With the recent high integration and speed increase of semiconductor devices or the like, the reduction of the resistance of wiring materials has become essential. Although various materials are available as the wiring materials, some wiring materials are difficult to process by dry etching. Therefore, a process by of depositing an insulating film on an underlayer wiring, forming contact holes and wiring channels in the insulating film, and depositing a conductive material in the contact holes and wiring channels has been adopted.

Replace the paragraph beginning at page 1, line 29 with:

Next, the filling material is subject to overall etching, such as reactive ion etching and ashing in <u>an</u> oxygen plasma, to leave the burying material only in the contact holes. Then, a resist having a pattern of wiring channels that overlap the contact holes is formed on the insulating film wherein the burying material is buried using a photolithography technique, and the burying material and the insulating film is etched to a predetermined depth using the resist as a mask to form wiring channels, which <u>is are</u> second depressed portions. At this time, since the under-layer wirings on the bottoms of the contact holes are covered with the burying material, etching does not damage the under-layer wirings. Furthermore, the resist and the burying material remaining after etching are removed to expose the under-layer wirings on the bottoms of the contact holes. Then, a conductive material is deposited in the contact holes and the wiring channels to form wirings in contact with the under-layer wirings (refer to e.g., Japanese Patent Laid-Open No. 8-335634 (p. 4, Fig. 1)).

Replace the paragraph beginning at page 2, line 24 with:

If the film of the burying material on the insulating film is removed by overall etching, such as reactive ion etching and ashing in an oxygen plasma, it is difficult to planarize the upper surfaces of the burying material in the contact holes and the insulating film in at the same level. There has been a problem in that even when the pattern for wiring channels overlaps the pattern for the contact holes, the pattern for highly accurate wiring channels cannot be formed, because the surface of the insulating film in this area cannot be planarized.

In re Appln. of ISHIBASHI et al. Application No. Unassigned

Replace the paragraph beginning at page 3, line 1 with:

Conventionally, an organic polymeric material functioning as an antireflective film has been used as the burying material. However, since this material contains aromatic compounds that absorb the light of at wavelengths used in photolithography, the material is cured, and the etching rate thereof becomes smaller than the etching rate of the insulating film. Consequently, the etching of the burying material buried in the contact holes is delayed, in etching for forming the wiring channel pattern, and the surrounding insulating film remains not etched. Therefore, there has been a problem of forming a fence-like etching residue on the edges of the contact holes after removing the burying material.

Replace the paragraph beginning at page 4, line 9 with:

Fig. 1-shows Figs. 1(A)-1(G) show a method for manufacturing a buried wiring structure according to the first embodiment of the present invention.

Replace the paragraph beginning at page 4, line 11 with:

Fig. 2 shows Figs. 2(A)-2(G) show a method for manufacturing a buried wiring structure according to the second embodiment of the present invention.

Replace the paragraph beginning at page 4, line 16 with:

Fig. 1 shows Figs. 1(A)-1(G) show a method for manufacturing a buried wiring structure according to the \underline{a} first embodiment of the present invention.

Replace the paragraph beginning at page 7, line 11 with:

Fig. 2shows Figs. 2(A)-2(G) show a method for manufacturing a buried wiring structure according to the <u>a</u> second embodiment of the present invention.